What is claimed is:

1. An ESD protection device comprising:
a substrate;
a first doped region formed in the substrate; and
a second doped region formed in the substrate and separated from the first doped region by only the substrate region, wherein the ESD protection device comprises no gate above the first and second doped regions.

2. The ESD protection device of claim 1, wherein the substrate comprises a first conductivity type and the first and second doped regions comprise a second conductivity type.

3. The ESD protection device of claim 1, wherein the substrate comprises a p-type conductivity material and the first and second doped regions comprise an n-type conductivity material.

4. The ESD protection device of claim 1, wherein first and second doped regions comprise a higher doping concentration than a doping concentration of the substrate.

5. The ESD protection device of claim 1 further comprising a first isolation structure placed on an opposing side of the first doped region from a region separating the first and the second doped regions, and a second isolation structure placed on an opposing side of the second doped region from a region separating the first and the second doped regions.

6. An ESD protection device comprising:
a substrate;
a first doped region formed in the substrate; and

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a second doped region formed in the substrate and separated from the first doped region by only the substrate region, wherein an amount current flowing between the first and second doped regions is not controlled by a voltage potential of a gate above the first and second doped regions.

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7. A gateless ESD protection device comprising:

a substrate;

a first doped region formed in the substrate; and

a second doped region formed in the substrate and separated from the first doped region by only the substrate region.

8. An ESD protection device comprising:

a substrate;

a first active region formed in the substrate; and

a second active region formed in the substrate and separated from the first active region by only the substrate region, wherein each of the first and second active regions includes a source/drain region, a LDD region and a halo region, wherein the LDD region surrounds the source/drain region and the halo region surrounds the LDD region, wherein the ESD protection device comprises no gate above the first and second active regions.

9. The ESD protection device of claim 8, wherein the substrate comprises a first conductivity type and the source/drain region comprises a second conductivity type.

10. The ESD protection device of claim 8, wherein the substrate comprises a p-type conductivity material and the source/drain region comprises an n-type conductivity material.

11. The ESD protection device of claim 9, wherein the LDD region comprises the same conductivity type as the conductivity type of the source/drain region, wherein a doping concentration of the LDD region is lower than a doping concentration of the source/drain region.

12. The ESD protection device of claim 9, wherein the halo region comprises the same conductivity type as the conductivity type of the substrate, wherein a doping concentration of the halo region is lower than a doping concentration of the substrate.

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13. An ESD protection device comprising:

a substrate; and

an implant within the substrate, the implant including two implant regions spaced apart by only the substrate region, wherein the substrate comprises a first conductivity type and the two implant regions comprise a second conductivity type, wherein conductivity between the two implant regions is not controlled by voltage potential of a gate above the two implant regions.

14. An ESD protection device comprising:

a substrate;

a first implant within the substrate, the first implant including two first doped regions spaced apart by only the substrate region, wherein the first implant comprises a first depth;

a second implant inside the two first doped regions, the second implant comprising a second depth, wherein the second depth is shallower than the first depth; and

a third implant inside the second implant, the third implant comprising a third depth, wherein the third depth is shallower than the second depth,

wherein the ESD protection device comprises no gate above the first, second and third implants.

15. An ESD protection device comprising:

a substrate;

a first active region formed in the substrate; and

a second active region formed in the substrate and separated from the first active region by only the substrate region, wherein each of the first and second active regions includes a source/drain region, wherein the first active region further includes an LDD region and a halo region, wherein the LDD region surrounds the source/drain region and the halo region surrounds the LDD region, wherein the ESD protection device comprises no gate above the first and second active regions.

16. An ESD protection device comprising:

a substrate;

a first active region formed in the substrate; and

a second active region formed in the substrate and separated from the first active region by only the substrate region, wherein the first active region includes an LDD region surrounded by a halo region, and an ohmic-contact region adjacent to the halo region, wherein the second active region include a source/drain region, wherein the ESD protection device comprises no gate above the first and second active regions.

17. An integrated circuit comprising:

a voltage source;

an external bonding pad; and

an ESD protection device connected between the bonding pad and the voltage source, the ESD protection device comprising:

a substrate;

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a first doped region formed in the substrate; and

a second doped region formed in the substrate and separated from the first doped region by only the substrate region, wherein the ESD protection device comprises no gate above the first and second doped regions.

18. The ESD protection device of claim 17, wherein the substrate comprises a first conductivity type and the first and second doped regions comprise a second conductivity type.

19. The ESD protection device of claim 17, wherein the substrate comprises a p-type conductivity material and the first and second doped regions comprise an n-type conductivity material.

20. The ESD protection device of claim 17, wherein first and second doped regions comprise a higher doping concentration than a doping concentration of the substrate.

21. The integrated circuit of claim 17, wherein the voltage source is connected to ground.

22. The integrated circuit of claim 17, wherein the voltage source is connected to a voltage supply.

23. An integrated circuit comprising:

a first voltage source;

a second voltage source;

an external bonding pad;

a first ESD protection device connected between the first voltage source and the external bonding pad; and

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a second ESD protection device connected between the second voltage source and the external bonding pad, wherein the second ESD protection device comprising:

a substrate;

a first doped region formed in the substrate; and

a second doped region formed in the substrate and separated from the first doped region by only the substrate region,

wherein the ESD protection device comprises no gate above the first and second doped regions.

24. The integrated circuit of claim 23, wherein the first voltage source is substantially smaller than the second voltage source.

25. The integrated circuit of claim 23, wherein the first voltage source is connected to ground.

26. The integrated circuit of claim 23, wherein the second voltage source is connected to a voltage supply.

27. An integrated circuit comprising:

a voltage source;

an external bonding pad;

an internal circuit connected to the external bonding pad at a node; and

an ESD protection device connected between the node and the voltage source,

the ESD protection device comprising:

a substrate;

a first doped region formed in the substrate; and

a second doped region formed in the substrate and separated from the first doped region by only the substrate region,

wherein the ESD protection device comprises no gate above the first and second doped regions.

28. An integrated circuit comprising:

a first voltage source;

a second voltage source;

an external bonding pad;

an internal circuit connected to the external bonding pad at a node;

a first ESD protection device connected between the first voltage source and the node; and

a second ESD protection device connected between the second voltage source and the node, wherein the second ESD protection device comprising:

a substrate;

a first doped region formed in the substrate; and

a second doped region formed in the substrate and separated from the first doped region by only the substrate region,

wherein the ESD protection device comprises no gate above the first and second doped regions.

29. A semiconductor chip comprising:

a package having a plurality of pins; and

an ESD protection device connected to at least one of the pins, the protection device comprising:

a substrate;

a first doped region formed in the substrate; and

a second doped region formed in the substrate and separated from the first doped region by only the substrate region,

wherein the ESD protection device comprises no gate above the first and second doped regions.

30. A method of producing a semiconductor device, the method comprising:

masking a substrate with a resist; and

forming a first and a second doped region in the substrate, wherein the first and second doped regions are separated by only the substrate, wherein a spacing between the first and second doped regions is defined by a length of the resist, wherein forming the first and second doped regions includes not forming a gate above the first and second doped regions.

31. A method of producing an ESD protection device, the method comprising:

masking a substrate with a resist to form a first and second unmasked regions of the substrate, wherein the unmasked regions are separated by a length of the resist;

implanting dopants into the first and second unmasked regions to form a first and second source/drain regions; and

removing the resist without forming gate above the first and second source/drain regions.

32. A method of forming a semiconductor device, the method comprising:

providing a substrate having no gate structure on the substrate;

masking the substrate with a resist to define a first and second unmasked regions, the first and second unmasked regions being separated by a distance, wherein the distance equals the length of the resist; and

implanting dopants into the first and second unmasked regions; and

removing the resist.

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